REMARKS

At the time of the Office Action dated June 4, 2003, claims 1-4 and 6-13 were pending in this application. Of those claims, claims 1-2, 4 and 10-13 have been rejected. Applicant acknowledges, with appreciation, the Examiner's indication that claims 3 and 6-9 contain allowable subject matter, and claims 1 and 10-11 have been amended, and care has been exercised to avoid the introduction of new matter. Specifically, claims 10 and 11 have been amended to address informalities. Claim 1 has been amended to clarify that a second buried impurity region of a second conductive type is vertically positioned between said first buried impurity region and said semiconductor layer relative to the substrate. Applicant submits that the present Amendment does not generate any new matter issue.

On page four of the Office Action, the Examiner objected to claims 10 and 11 for various informalities. In particular, the Examiner asserted that the phrase "said second buried impurity region" in claim 10 should be replaced by "said buried impurity region" and the phrase "said first impurity region" in claim 11 should be replaced by "said second impurity region." In response, Applicant notes that claims 10 and 11 have been amended, as suggested by the Examiner. Applicant, therefore, respectfully solicits withdrawal of the objections to claims 10 and 11.

Claims 10-13 are rejected under the first paragraph of 35 U.S.C. § 112

On pages four and five of the Office Action, the Examiner asserted that claims 10-13 contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. This rejection is respectfully traversed.

In the statement of the rejection, the Examiner asserted:

> In particular, the only conductivity type for said buried impurity region that comes into consideration is n-type, because none of the p-type buried impurity regions are formed in between the semiconductor substrate 1 and the semiconductor layer 2. However, none of the Figures 1-29 show said n-type buried impurity layer to be in electrical contact with any impurity region of the same (first) conductivity type with said impurity region of the same (first) conductivity type being formed on the surface of said semiconductor layer 2.

Applicant respectfully disagrees. All of the features recited in claim 10 are supported by Fig. 25 except for a gap part in the buried impurity region 3. Fig. 25 is described in Applicant's specification as illustrating the tenth embodiment of the invention (page 22, lines 24-27). Referring to page 25, lines 16-19 of Applicant's specification, it is stated:

> Here, though the case wherein narrowed parts are formed in the N+ buried diffusion region is described in the tenth and eleventh embodiments, the structure where slits with proper intervals are provided can improve the withstanding voltage in the same manner.

Thus, the specification clearly states that slits can replace the narrowed parts in the N+ buried diffusion region (i.e., the claimed buried impurity region) of the tenth embodiment. Slits are described throughout the specification, for example, page 12, lines 20-23 and Fig. 7, with the disclosed slits being comparable to the claimed gap part. Furthermore, it is clear from Fig. 25 that the first impurity region 36 is electrically connected to the buried impurity region 3. Thus, Applicant respectfully submits that the specification fully supports these limitations in such a way as to enable one skilled in the art to make and/or use the invention.

Claims 1, 4, 10 and 12-13 are rejected under 35 U.S.C. § 102 for lack of novelty based upon Mosher et al., U.S. Patent No. 5,256,582 (hereinafter Mosher)

On pages six through ten of the Office Action, the Examiner referred particularly to Fig. 11 and asserted that Mosher identically discloses the invention as claimed. This rejection is respectfully traversed.

Independent claim 1, as amended, recites that a second buried impurity region of a second conductive type is vertically positioned relative to the substrate between a first buried impurity region and a semiconductor layer. In the statement of the rejection, the Examiner referred to feature 24 as the claimed first buried impurity region, feature 42 as the claimed second buried impurity region, and feature 52 as the claimed semiconductor layer. Referring to Fig. 11 of Mosher, feature 42 is not vertically positioned relative to the substrate between feature 24 and feature 52. Therefore, Mosher fails to identically disclose the claimed invention, as recited in claim 1, within the meaning of 35 U.S.C. § 102.

With regard to claim 10, the Examiner stated that the "claimed electrical connection is undisclosed by Applicant, see rejection under [sic] U.S.C. 112, first paragraph, as included above." Although not explicitly stated, the Examiner believed this alleged non-disclosure of the claimed feature that the first impurity region is electrically connected to the buried impurity region need not be disclosed. This, however, does not comport with law regarding 35 U.S.C. § 102, which requires an Examiner establish that an applied reference disclose each limitation of the claimed invention. Notwithstanding, the Examiner identified feature 24 as the claimed buried impurity region and feature 79 as the first impurity region, but as clearly illustrated in Fig. 11 of Mosher, feature 24 is not electrically connected to feature 79. Thus, Mosher fails to identically disclose the claimed invention, as recited in claim 10, within the meaning of 35 U.S.C. § 102. Applicant, therefore, respectfully solicits withdrawal of the imposed rejection of claims 1, 4, 10 and 12-13 under 35 U.S.C. § 102 for lack of novelty based upon Mosher.

Claims 2 and 11 are rejected under 35 U.S.C. § 103 for obviousness based upon Mosher in view of Isaac et al., U.S. Patent No. 4,495,512 (hereinafter Isaac)

In the statement of the rejection, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify Mosher in view of Isaac to change the conductivity type of the third region 55. This rejection is respectfully traversed.

Claims 2 and 11, respectively, depend from independent claims 1 and 10, and Applicant incorporates herein the arguments previously advanced in traversing the imposed rejection of claims 1 and 10 under 35 U.S.C. § 102 for lack of novelty as evidenced by Mosher. Specifically, Mosher neither discloses nor suggests a second buried impurity region of a second conductive type that is vertically positioned relative to the substrate between a first buried impurity region and a semiconductor layer, as recited in claim 1, or a first impurity region that is electrically connected to a buried impurity region, as recited in claim 10. The secondary reference to Isaac does not cure these argued deficiencies of Mosher. Accordingly, the proposed combination of references would not yield the claimed invention. Applicant, therefore, respectfully submits that the imposed rejection of claim 2 and 11 under 35 U.S.C. § 103 for obviousness based upon Mosher in view of Isaac is not viable and, hence, solicits withdrawal thereof.

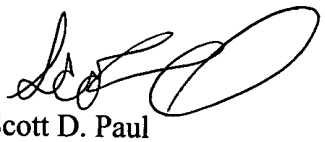
Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing

remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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